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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, JIMMY H	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/721,250	JEOUNG ET AL.	
	Examiner	Art Unit	
	Jimmy H. Nguyen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-11,13-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-11,13-18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/09/2007 has been entered. Claims 1-5, 7-11, 13-18 and 20 are currently pending in the application. An action follows below:

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1-5, 7, 9-11, 13, 15, 16, 18 and 20** are rejected 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art, hereinafter AAPA, and further in view of Maekawa et al. (US 5,764,207), hereinafter Maekawa.

As to **claims 1, 2 and 9**, the claimed invention reads on AAPA as follows: AAPA discloses a liquid crystal display (LCD) device (see Fig. 1; para [0004]) and an associate driving method (see Figs. 3-6), the LCD comprising **an LCD panel** (12; see Fig. 1) including a plurality of **gate lines (GL1-GLn**; see Fig. 1); a plurality of **data lines (signal lines DL1-DLm**; see Fig. 1) crossing the plurality of gate lines (GL1-GLn); and a plurality of **liquid crystal cells (20**; see Fig. 1) arranged at crossings of plurality of gate and data lines (see Fig. 1); and **a LCD panel driver (14, 16, 18**; see Fig. 1) including **a gate driver (14**; see Fig. 1) sequentially driving gate

lines (G) during the **data apply period (DAP**; see Figs. 3-5) and **a data driver (16**; see Fig. 1) applying effective pixel signals (see Figs. 3-4) to the plurality of data lines (DL) during the data apply period (DAP) and placing the data lines in floating state during a **blanking period (BP**; Figs. 3-4) following the data apply period (see Figs. 3-4). AAPA further teaches **a frame (1F**; Figs. 3-4) including the data apply period (DAP) and the blanking period (BP) (Figs. 3-4; para [0019],[0020]). AAPA does not expressly teach limitations, "the data driver applying dummy pixel signals during the blanking period" and "polarities of the dummy pixel signal applicable to adjacent ones of data lines of the plurality of data lines are invertable by the data driver during the blanking period" as presently claimed. Accordingly, AAPA discloses all limitations of these claims except for the above underlined limitations.

However, Maekawa display a related LCD device (see Fig. 3) comprising a data driver (a driver including elements 13, inverters, NAND gates, switches HSW; see Fig. 3) applying effective pixel signals (actual video signals during actual video period; see waveform VSIG of Fig. 4) to the plurality of data lines during the data apply period (the actual video period; see Fig. 4) and dummy pixel signals representing a predetermined brightness level (signals with a predetermined potential level Vp; see Fig. 4) to the data lines during the blanking period (see Fig. 4, waveform of VSIG during a blanking period; col. 6, lines 19-22). Maekawa further teaches that polarities of the dummy pixel signals and the effective pixel signals are invertable together by the data driver in order to cause its polarity to be coincided with the video signal reversed (see col. 2, lines 41-46; col. 6, lines 19-27), thereby performing a restriction of a potential oscillation in the video line generated as the sampling rate of the video signal is increased (see col. 2, lines 17-21). Further, see Figs. 2 and 6 and the corresponding description.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to modify the data driver of AAPA to provide the dummy pixel signal during the blanking period, in view of the teaching in the Maekawa reference, because this would perform a restriction of a potential oscillation in the video line generated as the sampling rate of the video signal is increased, as taught by the Maekawa reference (see col. 2, lines 17-21).

As to **claim 3**, AAPA teaches the effective pixel signals comprising analog signals converted by the data driver (16) from digital pixel data applied from a timing controller (18) controlling the gate driver (14) and the data driver (16) during the data apply period (see para [0009]-[0010]).

As to **claim 4**, Maekawa teaches the video signal (VID) including the effective pixel signal and dummy pixel signal) and provided from the timing controller (a signal driver 3; see Fig. 1). AAPA teaches the digital video signal provided from the timing controller (page 5, lines 4-16). Accordingly, AAPA in view of Maekawa discloses limitations of this claim.

As to **claim 10**, Maekawa discloses that after a fixed potential applied to all signal lines during D1-DN ON, all switches HSWs are in OFF condition, thereby rendering all signal lines being floated (see Fig. 6).

As to **claims 15 and 16**, since these claims similarly recite the limitations of claim 10, these claims are therefore rejected for the same reason set in claim 10.

As to **claims 5, 7, 11, 13, 18 and 20**, AAPA discloses all limitations of these claims (see Figs. 3-6).

4. Claims **1-5, 7-11, 13-18 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Suzuki et al. (US 5,598,180), hereinafter Suzuki, and further in view of Maekawa.

As to claims **1, 2, 8, 9 and 14**, the claimed invention reads on AAPA as follows: AAPA discloses a liquid crystal display (LCD) device (see Fig. 1; para [0004]) and an associate driving method (see Figs. 3-6), the LCD comprising **an LCD panel** (12; see Fig. 1) including a plurality of **gate lines (GL1-GLn**; see Fig. 1); a plurality of **data lines (signal lines DL1-DLm**; see Fig. 1) crossing the plurality of gate lines (GL1-GLn); and a plurality of **liquid crystal cells (20**; see Fig. 1) arranged at crossings of plurality of gate and data lines (see Fig. 1); and **a LCD panel driver (14, 16, 18**; see Fig. 1) including **a gate driver (14**; see Fig. 1) sequentially driving gate lines (G) during the **data apply period (DAP**; see Figs. 3-5) and **a data driver (16**; see Fig. 1) applying effective pixel signals (see Figs. 3-4) to the plurality of data lines (DL) during the data apply period (DAP) and placing the data lines in floating state during a **blanking period (BP**; Figs. 3-4) following the data apply period (see Figs. 3-4). AAPA further teaches **a frame (1F**; Figs. 3-4) including the data apply period (DAP) and the blanking period (BP) (Figs. 3-4; para [0019],[0020]). AAPA does not expressly teach limitations, "the data driver applying, during the blanking period, dummy pixel signals comprising white signals" and "polarities of the dummy pixel signal applicable to adjacent ones of data lines of the plurality of data lines are invertable by the data driver during the blanking period", as presently claimed. Accordingly, AAPA discloses all limitations of these claims except for the above underlined limitations.

However, Suzuki discloses an active matrix LCD comprising a control circuit inputting white-level signal (i.e., the claimed dummy pixel signal) to signal-line drive IC circuit, which

applies a white-level (predetermined brightness level) potential to each signal line during the blanking period, in order to ensure no image being displayed during the blanking period (see col. 8, lines 18-25). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to modify the data driver of AAPA to provide white dummy pixel signal during the blanking period, in view of the teaching in the Suzuki reference, because this would ensure unwanted image being displayed during the blanking period, as taught by Suzuki, thereby improve the image quality.

Accordingly, AAPA in view of Suzuki discloses all limitations of these claims except that polarities of the dummy pixel signal applicable to adjacent ones of data lines of the plurality of data lines are invertable by the data driver during the blanking period.

However, Maekawa display a related LCD device (see Fig. 3) comprising a data driver (a driver including elements 13, inverters, NAND gates, switches HSW; see Fig. 3) applying effective pixel signals (actual video signals during actual video period; see waveform VSIG of Fig. 4) to the plurality of data lines during the data apply period (the actual video period; see Fig. 4) and dummy pixel signals representing a predetermined brightness level (signals with a predetermined potential level Vp; see Fig. 4) to the data lines during the blanking period (see Fig. 4, waveform of VSIG during a blanking period; col. 6, lines 19-22). Maekawa further teaches that in order to carry out an AC driving (i.e., inversion driving method), **polarities of the dummy pixel signals and the effective pixel signals are invertable together** by the data driver in order to cause its polarity to be coincided with the video signal reversed (see col. 2, lines 41-46; col. 4, line 65 through col. 5, line 4; col. 6, lines 19-27), thereby performing a restriction of a potential oscillation in the video line generated as the sampling rate of the video signal is

increased (see col. 2, lines 17-21). Furthermore, the LCD device of AAPA is driven by a dot-inversion driving method (see Figs. 3-5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to modify the data driver of AAPA in view of Suzuki to invert the polarities of the dummy pixel signal applicable to adjacent ones of data lines of the plurality of data lines during the blanking period, in view of the teaching in the Maekawa reference, because this would perform a restriction of a potential oscillation in the video line generated as the sampling rate of the video signal is increased, as taught by the Maekawa reference (see col. 2, lines 17-21).

As to **claim 3**, AAPA teaches the effective pixel signals comprising analog signals converted by the data driver (16) from digital pixel data applied from a timing controller (18) controlling the gate driver (14) and the data driver (16) during the data apply period (see para [0009]-[0010]).

As to **claim 4**, Maekawa teaches the video signal (VID) including the effective pixel signal and dummy pixel signal) and provided from the timing controller (a signal driver 3; see Fig. 1). AAPA teaches the digital video signal provided from the timing controller (page 5, lines 4-16). Accordingly, AAPA in view of Maekawa discloses limitations of this claim.

As to **claim 10**, Maekawa discloses that after a fixed potential applied to all signal lines during D1-DN ON, all switches HSWs are in OFF condition, thereby rendering all signal lines being floated (see Fig. 6).

As to **claims 15 and 16**, since these claims similarly recite the limitations of claim 10, these claims are therefore rejected for the same reason set in claim 10.

As to **claims 5, 7, 11, 13, 18 and 20**, AAPA discloses all limitations of these claims (see Figs. 3-5).

As to **claim 17**, see the rejection to claims 8 and 14 above.

Response to Arguments

5. Applicant's arguments filed 10/09/2007 have been fully considered but they are **not fully persuasive**.

Applicant's argument, see page 7 of the amendment, filed 10/09/2007, with respect to the rejection under 35 USC 112, second paragraph, to claims 1-5, 7 and 8, in the Office Action dated 7/10/2007, has been fully considered and is persuasive in light of the amendment to independent claim 1. The rejection under 35 USC 112, second paragraph, to claims 1-5, 7 and 8, in the Office Action dated 7/10/2007, has been withdrawn.

Applicant argues that none of the cited references teaches "wherein a frame includes the data apply period and the blacking period" newly added to all independent claims 1, 9 and 15; see pages 7-8 of the amendment, filed 10/09/2007. Examiner directs the Applicant to either the detailed rejections above or Figs. 3-5 of AAPA, where AAPA explicitly teaches the above underlined limitation.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy H. Nguyen whose telephone number is 571-272-7675. The examiner can normally be reached on Monday - Friday, 6:30 a.m. - 3:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached at 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JHN
December 30, 2007

Jimmy H. Nguyen
Primary Examiner
Art Unit: 2629